Reg. No. : .....

Name : .....

GOVERNMENT COLLEGE LIBRARY KASARAGOD

K18U 0510

II Semester B.Sc. Degree (CBCSS-Reg./Supple./Imp.)
Examination, May 2018
CORE COURSE IN PHYSICS
2B02 PHY : Electronics – I
(2014 Admn. Onwards)

Time : 3 Hours Max. Marks : 40

***Instruction** : Write answers in English **only**.*

SECTION – A

(Answer **all**-Very short answer type-**Each** question carries **one** mark.)

1. The point of intersection of dc and ac load line represents _____
2. A JFET is a _____ driven device.
3. The 8 bit binary equivalent of $(187)_{10}$ is _____
4. NAND gate is known as _____ gate. **(4×1=4)**

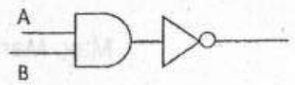
SECTION – B

(Answer **any seven**-Short answer type-**Each** question carries **two** marks.)

5. Common collector circuit is known as emitter follower. Comment on it.
6. What is stabilization of operating point ? What is its need ?
7. Define α. Show that α is always less than unity.
8. Why JFET is known as unipolar transistor ?
9. List any four advantages of JFET.

P.T.O.

10. Define the following terms
    i) Shorted gate drain current
    ii) Pinch off voltage.
11. What are the three basic logic gates ?
12. What is the Boolean equation for the output of figure below ? What is the output if one input is high ?



13. Convert the decimal number 46 into binary equivalent.
14. Explain the signed magnitude scheme with an example. **(7×2=14)**

SECTION – C

(Answer **any four**-short essay/problem type-**Each** question carries **three** marks.)

15. The collector leakage current in a transistor is 250 μ A in CE arrangement. If the transistor is connected in CB arrangement, what will be the leakage current.
16. In a Common Base connection α=0.95. The voltage drop across 2kΩ resistance which is connected in the collector is 2V. Find the base current.
17. What are the JFET parameters ? Obtain a relation between them.
18. In an n-channel JFET biased by potential divider method, it is desired to set the operating point at I_D=2.5 mA and V_{DS} = +8 V. If V_{DD}=30V, R_1 = 1MΩ and R_2 = 500 KΩ . Find the values of R_s. The parameters of JFET are IDSS = 10MA and VGS (off) = –5V.
19. State and prove de-Morgan's theorem.
20. Subtract 7 from 18 by two's complement method. **(4×3=12)**

SECTION – D

(Answer **any two**-Long essay type-**Each** question carries **five** marks.)

21. Describe the potential divider method in detail. Derive an expression for stability factor.
22. Explain the construction and working of a JFET.
23. Explain combinational logic circuits using NAND and NOR gates.
24. What are binary coded decimals ? How two BCD numbers are arithmetically operated ? **(2×5=10)**

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