Reg No:..... K25FY2471 C
Name :.....

Second Semester FYUGP Physics Examination
APRIL 2025 (2024 Admission onwards)
KU2DSCPHY125 (DIGITAL ELECTRONICS)
(DATE OF EXAM : 02-05-2025)

Time : 90 min Maximum Marks : 50

Part A (Answer any 6 questions. Each carries 2 marks)

1. Convert the binary number 11101 to decimal. 2

2. Convert the decimal number 59 to binary using repeated division by 2 2

3. Convert the decimal number -18 into a signed 2's complement representation. 2

4. Name two advantages of digital data compared to analog data 2

5. What is distributive law of Boolean algebra? 2

6. Determine the values of A and B that make the sum term $\overline{A} + B = 0$. 2

7. Write the standard product term for each cell in a 3-variable Karnaugh map. 2

8. Implement AB using two NAND gates. 2

Part B (Answer any 4 questions. Each carries 6 marks)

9. Convert the following hexadecimal number to decimal:
   (a) $8D_{16}$
   (b) $F3_{16}$ 6

10. Explain the process of finding the 2's complement of a binary number and verify it using an example. 6

11. List the sequence of levels(HIGH and LOW) that represent each of the following bit sequence 1011101, 11101001, 100110 6

12. Apply DeMorgan's theorems to each of the following expressions:

    (a) $\overline{(A + B + C)D}$
    (b) $\overline{ABC + DEF}$

    6

13. Convert the following expressions to an equivalent SOP/POS expression:

    a) $\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}C + ABC$

    b) $(A + \bar{B} + C)(A + B + \bar{C})$ 6

14. Explain briefly how NAND gate acts as a universal logic element. 6

Part C (Answer any 1 question(s). Each carries 14 marks)

15. Explain one application of i)OR gate ii) NAND gate iii) NOR gate. 14

16. (a) 1100 and 1100 is added with a 4bit parallel adder with input carry 0.Find the sum.Show the details of your work 7
    (b) Explain the working of 4bit comparator with logic symbol 7