Reg No:.....
Name :.....

K25FY2471 B

Second Semester FYUGP Physics Examination
APRIL 2025 (2024 Admission onwards)
KU2DSCPHY125 (DIGITAL ELECTRONICS)
(DATE OF EXAM: 30-4-2025)

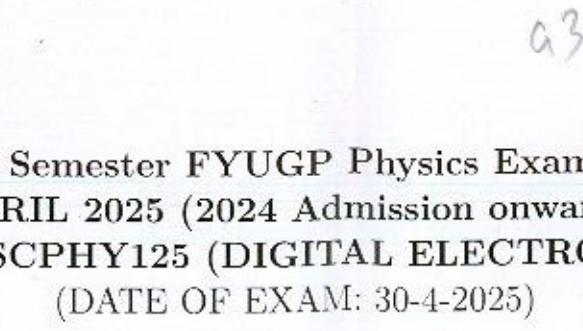
Time : 90 min | Maximum Marks : 50

Part A (Answer any 6 questions. Each carries 2 marks)

1. In the octal number system, write the four numbers that come after 7? 2
2. What is Binary Coded Decimal (BCD) 2
3. What is the weight of each 1 in BCD number 1000? 2
4. Determine the total number of possible input combinations for a 4-input AND gate. 2
5. A device is needed to indicate when two LOW levels occur simultaneously on its inputs and to produce a HIGH output as an indication. Specify the device. 2
6. State DeMorgan's second theorem? 2
7. Express A+ B using three NAND gates. 2
8. What you mean by a full adder 2

Part B (Answer any 4 questions. Each carries 6 marks)

9. Convert each decimal number to octal by repeated division by 8:
   (a) 359
   (b) 439 6
10. Explain the difference between positive and negative logic 6
11. How does an exclusive - OR gate differ from an OR gate in its logical operation? 6
12. The Boolean expression for an exclusive-OR gate is AB+AB. With this as a starting point, use DeMorgan's theorems and any other rules or laws that are applicable to develop an expression for the exclusive-NOR gate. 6
13. Implement X= AB+CD using NAND gates. 6
14. For the parallel adder in figure determine the complete sum by the analysis of the logical operations of the circuit.Verify the result by the direct addition of the two input numbers 6



Part C (Answer any 1 question(s). Each carries 14 marks)

15. (a) Given an 8-bit binary number 10111010_2, find its 1's complement and 2's complement, then determine its decimal equivalent. 7
    (b) Compare Signed Magnitude, 1's Complement, and 2's Complement representations of negative numbers. Give an example of each and explain their advantages and disadvantages. 7
16. Determine which of the logic circuits in figure are equivalent 14